IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG.PHILIPS LCD CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; TATUNG COMPANY; TATUNG COMPANY OF AMERICA, INC.; AND VIEWSONIC CORPORATION, Defendants.	Civil Action No. _____ DEMAND FOR TRIAL BY JURY

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff LG.Philips LCD Co., Ltd. ("LG.Philips") for its Complaint against Defendants Chi Mei Optoelectronics Corporation; AU Optronics Corporation; AU Optronics Corporation America; Tatung Company; Tatung Company of America, Inc.; and ViewSonic Corporation (collectively the "Defendants") for injunctive and declaratory relief and for damages, including treble or multiple damages, for patent infringement, states and alleges as follows:

NATURE OF THE ACTION

1. LG.Philips is the owner of United States Patent No. 5,019,002 ("the '002 Patent"), United States Patent No. 5,825,449 ("the '449 Patent"), and United States Patent No. 4,624,737 ("the '737 Patent") (collectively the "Patents-in-Suit").

2. This is a civil action for the infringement of the Patents-in-Suit, including the willful infringement of the Patents-in-Suit by Defendants.

3. The technology at issue involves the design and manufacture of Liquid Crystal Display modules ("LCDs"), which are a type of flat panel display that are incorporated into at least LCD portable computers, LCD computer monitors, and LCD televisions.

THE PARTIES

4. Plaintiff LG.Philips is a corporation organized under the laws of the Republic of Korea, having a place of business located in Seoul, Korea.

5. Defendant Chi Mei Optoelectronics Corporation ("Chi Mei") is a Taiwanese corporation, having its principal place of business at 2F, No. 1, Chi-Yeh Road, Tainan Science Based Industrial Park, Hsinshih Hsiang, Tainan Hsien 710, TAIWAN 74147, R.O.C. Chi Mei manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

6. Defendant AU Optronics Corporation ("AUO") is a Taiwanese corporation, having its principal place of business at 1, Li-Hsin Rd., II, Science-Based Industrial Park, Hsinchu City 30077 Taiwan, ROC. AUO manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various

third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

7. Defendant AU Optronics Corporation America a/k/a AU Optronics America, Inc. ("AUO America") is a domestic subsidiary of AUO that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. AUO America is a California corporation, having its principal place of business at 1800 Wyatt Drive, Suite 7, Santa Clara, CA 95054. AUO America markets and sells AUO's products throughout the United States.

8. Defendant Tatung Company ("Tatung") is a Taiwanese corporation, having a place of business at 22 Chungshan N Rd. Section 3, Taipei, Taiwan. Tatung assembles LCD products in Taiwan and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

9. Defendant Tatung Company of America, Inc. ("Tatung America") is a domestic subsidiary of Tatung that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. Tatung America is a California corporation, having a place of business at 2850 El Presidio Street, Long Beach, California 90810. Tatung America markets and sells Tatung's products throughout the United States.

10. Defendant ViewSonic Corporation ("ViewSonic") is a Delaware Corporation, having a place of business at 381 Brea Canyon Road, Walnut, California 91789, which either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States,

JURISDICTION AND VENUE

11. This action is based upon and arises under the Patent Laws of the United States, 35 U.S.C. § 100 *et seq*., and in particular §§ 271, 281, 283, 284 and 285, and is intended to redress infringement of the Patents-in-Suit owned by LG.Philips.

12. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

13. Defendants have transacted and continue to transact business in the United States and in this judicial district by: using or causing to be used; making; importing or causing to be imported; offering to sell or causing to be offered for sale; and/or selling or causing to be sold directly, through intermediaries and/or as an intermediary, a variety of products that infringe the Patents-in-Suit to customers in the United States, including customers in this judicial district, and Defendants will continue to do so unless enjoined by this Court.

14. This Court has personal jurisdiction over Chi Mei, AUO, and Tatung, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c) and (d), and 28 U.S.C. § 1400(b), in that these Defendants are committing and are causing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary, and in that these Defendants have caused and cause injury and damages

in this judicial district by acts or omissions outside of this judicial district, including but not limited to utilization of their own distribution channels established in the United States and AUO America's and Tatung America's distribution channels in the United States, as set forth below, to ship a variety of products that infringe the Patents-in-Suit into the United States and into this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

15. This Court has personal jurisdiction over AUO America and Tatung America and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that these Defendants are committing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary. AUO America and Tatung America regularly import large quantities of AUO, and Tatung LCD products into the United States for distribution throughout the United States, including in this judicial district. AUO America and Tatung America are involved in the distribution of infringing LCD products and are aware that their products are sold throughout the United States, including in Delaware. The established distribution networks of these Defendants consist of national distributors and resellers, and these Defendants distribute to national retailers that have stores located in Delaware. By shipping into, offering to sell in, using, or selling products that infringe the Patents-in-Suit in this judicial district, or by inducing or causing those acts to occur, AUO America and Tatung America have transacted and transact business and perform works and services in this judicial district, have contracted and contract to supply services and things

in this judicial district, have caused and cause injury and damages in this judicial district by acts and omissions in this judicial district, and have caused and cause injury and damages in this judicial district by acts or omissions outside of this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

16. This Court has personal jurisdiction over ViewSonic, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that ViewSonic is incorporated and therefore resides in Delaware for purposes of establishing venue in this district, in that ViewSonic has been doing business in Delaware, including the infringing acts alleged herein, both directly, through one or more intermediaries, and/or as an intermediary, and will continue to do so unless enjoined by this Court.

THE PATENTS-IN-SUIT

17. On May 28, 1991, the '002 Patent, entitled "Method of Manufacturing Flat Panel Backplanes including Electrostatic Discharge Prevention and Displays Made Thereby," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '002 Patent. A copy of the '002 Patent is attached as Exhibit A.

18. On October 20, 1998, the '449 Patent, entitled "Liquid Crystal Display Device and Method of Manufacturing the Same," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '449 Patent. A copy of the '449 Patent is attached as Exhibit B.

19. On November 25, 1986, the '737 Patent, entitled "Process for Producing Thin-Film Transistor," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '737 Patent. A copy of the '737 Patent is attached as Exhibit C.

20. LG.Philips owns the Patents-in-Suit and possesses the right to sue and to recover for infringement of the Patents-in-Suit.

21. Defendants have been and are infringing and/or inducing infringement of the Patents-in-Suit because they at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in this judicial district and elsewhere in the United States products that infringe the Patents-in-Suit.

FACTUAL BACKGROUND

22. LG.Philips has invested substantial time and money in designing, developing, manufacturing and producing LCD products that incorporate the patented LCD technology.

23. LG.Philips derives substantial benefits from the exploitation of its patented technology in the United States and abroad. LG.Philips' interests, including, but not limited to, these benefits have been and continue to be harmed by the Defendants' infringement of the Patents-in-Suit.

24. The Defendants at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in the United States and in this judicial district LCDs and/or LCD products that are encompassed by and/or made by the methods claimed in the Patents-in-Suit.

25. The Defendants have induced and/or continue to induce the infringement of the Patents-in-Suit in the United States and in this judicial district.

26. Defendants maintain and develop relationships with business partners, including, for example, suppliers and customers, to promote and encourage the import, offering for sale, sale and use of its infringing visual display products in the United States.

27. Defendants actively sell to and solicit business from customers and distributors located in the United States. Defendants coordinate with these and other third parties concerning the designs, specifications, distribution and/or placement of orders regarding such LCDs and LCD products destined for the U.S. market.

28. Defendants also communicate with third parties to promote and encourage the use, sale, importation and/or offering for sale of these same LCDs and LCD products in and into the United States.

29. Defendants have relationships with third parties to develop and supply the U.S. market with such LCDs and LCD products.

30. Defendants communicate and meet with third parties about their LCDs and LCD products and these communications and meetings facilitate the sale, offer for sale and/or distribution of Defendants' LCDs and LCD products to customers and users in the United States.

COUNT I
INFRINGEMENT OF THE '002 PATENT

31. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

32. Defendants have infringed, and/or induced infringement of the '002 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that infringes one or more claims of the '002 Patent in this judicial district and elsewhere in the United States.

33. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '002 Patent, either literally or equivalently.

34. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '002 Patent and is without adequate remedy at law.

35. Defendants have, upon information and belief, infringed and are infringing the '002 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT II
INFRINGEMENT OF THE '449 PATENT

36. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

37. Defendants have infringed and/or induced infringement of the '449 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale,

selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that infringes one or more claims of the '449 Patent in this judicial district and elsewhere in the United States.

38. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '449 Patent, either literally or equivalently.

39. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '449 Patent and is without adequate remedy at law.

40. Defendants have, upon information and belief, infringed and are infringing the '449 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT III
INFRINGEMENT OF THE '737 PATENT

41. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

42. Defendants have infringed and/or induced infringement of the '737 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that were

made by a method that infringed one or more claims of the '737 Patent in this judicial district and elsewhere in the United States.

43. The products made by the infringed method that were used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '737 Patent, either literally or equivalently.

44. LG.Philips has been injured by Defendants' infringement of the '737 Patent.

45. Defendants have, upon information and belief, infringed the '737 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct was lawful. Defendants' infringement has been willful and deliberate, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff LG.Philips prays for judgment as follows:

A. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic have infringed the Patents-in-Suit;

B. That Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit has been willful;

C. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and

those persons acting in concert or participation with any of them, are enjoined and restrained from continued infringement, including but not limited to using, making, importing, offering for sale and/or selling products that infringe, and from inducing the infringement of, the '002 Patent and '449 Patent, prior to their expiration, including any extensions;

D. That Chi Mei, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them deliver to LG.Philips all products that infringe the Patents-in-Suit for destruction at LG.Philips' option;

E. That LG.Philips be awarded monetary relief adequate to compensate LG.Philips for Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's acts of infringement of the Patents-in-Suit within the United States prior to the expiration of the Patents-in-Suit, including any extensions;

F. That any monetary relief awarded to LG.Philips regarding the infringement of the Patents-in-Suit by Defendants be trebled due to the willful nature of Chi Mei's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit;

G. That any monetary relief awarded to LG.Philips be awarded with prejudgment interest;

H. That this is an exceptional case and that LG.Philips be awarded the attorneys' fees, costs and expenses that it incurs prosecuting this action; and

I. That LG.Philips be awarded such other and further relief as this Court deems just and proper.

JURY DEMAND

Plaintiff demands a trial by jury of any and all issues triable of right by a jury.

December 1, 2006

THE BAYARD FIRM

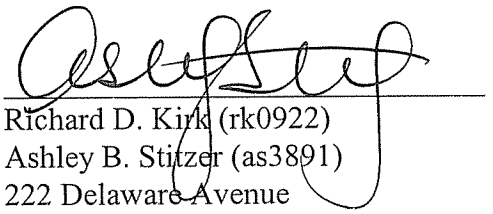

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EXHIBIT A

United States Patent [19]

Holmberg

[11] **Patent Number: 5,019,002**

[45] **Date of Patent: May 28, 1991**

[54] **METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY**

[75] Inventor: **Scott H. Holmberg**, San Ramon, Calif.

[73] Assignee: **Honeywell, Inc.**, Minneapolis, Minn.

[21] Appl. No.: **218,312**

[22] Filed: **Jul. 12, 1988**

[51] **Int. Cl.**[5] **H01L 45/00**

[52] **U.S. Cl.** **445/24**; 357/23.13; 437/56

[58] **Field of Search** 445/24, 3; 357/23.13, 357/4; 437/4, 8, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,455,739	6/1984	Hynecek	427/8 X
4,586,242	5/1986	Harrison	437/8
4,714,949	12/1987	Simmons et al.	357/23.13
4,736,271	4/1988	Mack et al.	357/23.13
4,803,536	2/1989	Tuan	357/23.13

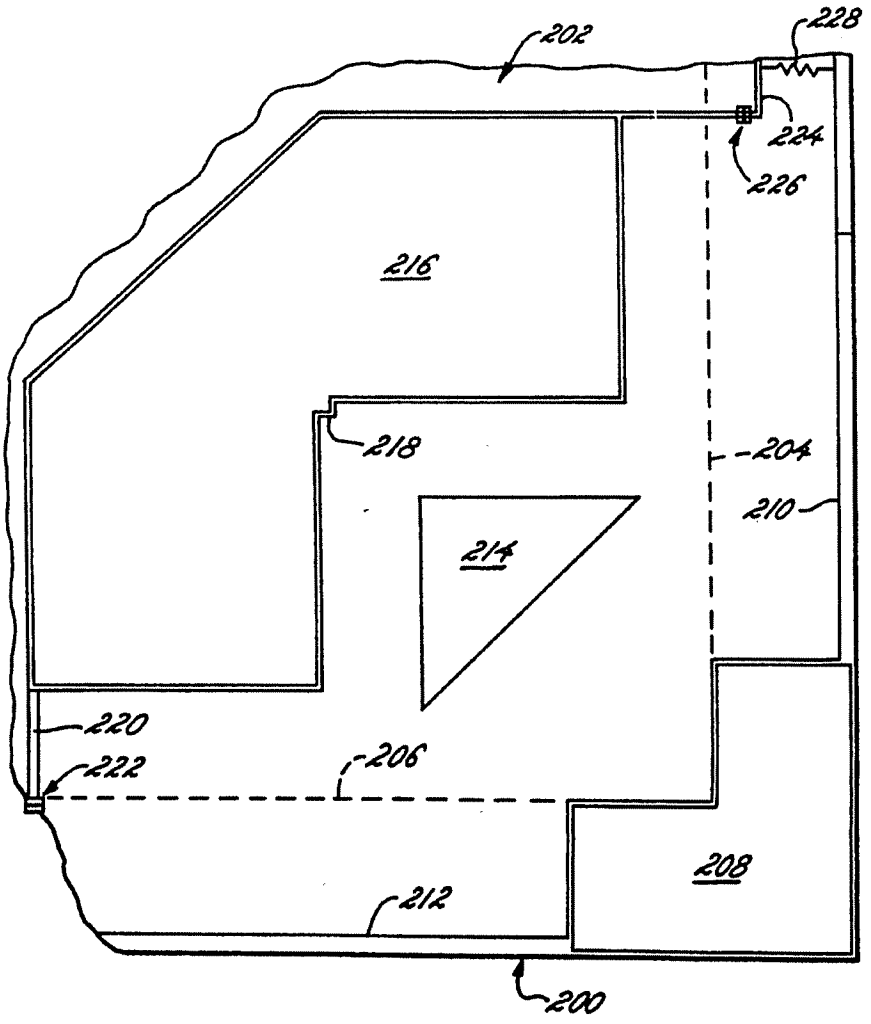
Primary Examiner—Kenneth J. Ramsey

Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

Flat panel displays are provided including protection from electrostatic discharge (ESD) during manufacture and thereafter. At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines. An internal ESD guard ring is coupled to the row and column lines via shunt transistors. An external ESD guard ring is coupled to the row and column lines via a resistance. Both of the guard rings can be provided; however, the external guard ring is removed prior to completion of the display.

36 Claims, 5 Drawing Sheets



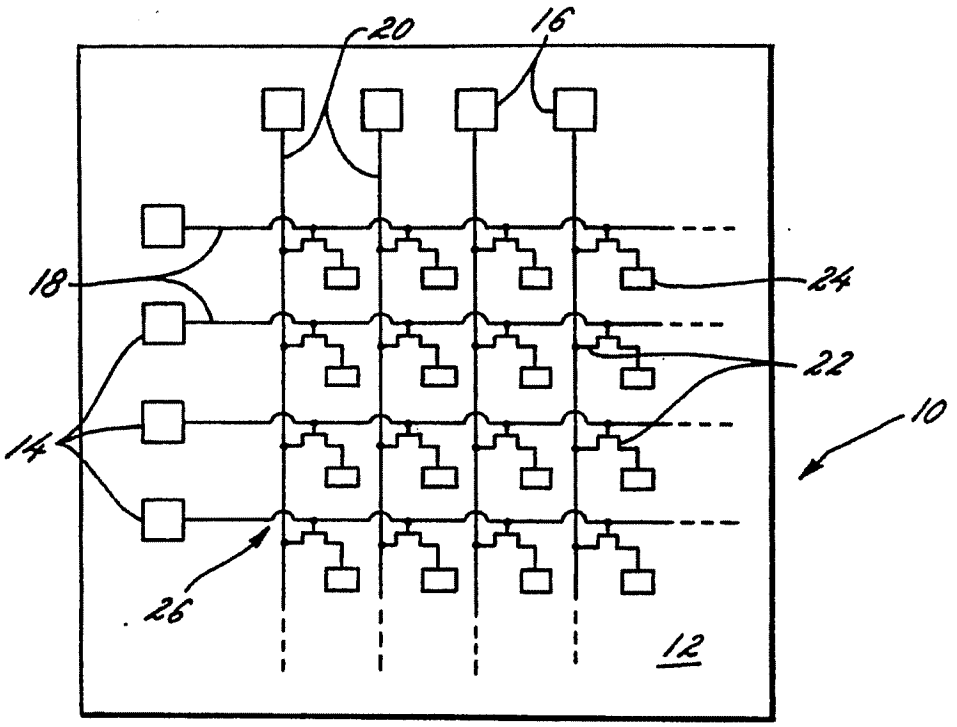


FIG. 1

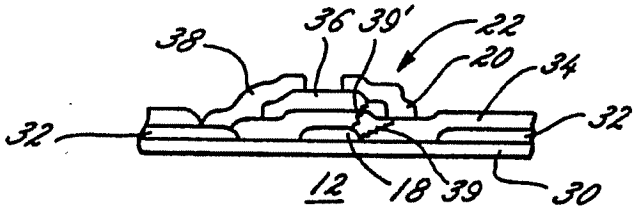


FIG. 2

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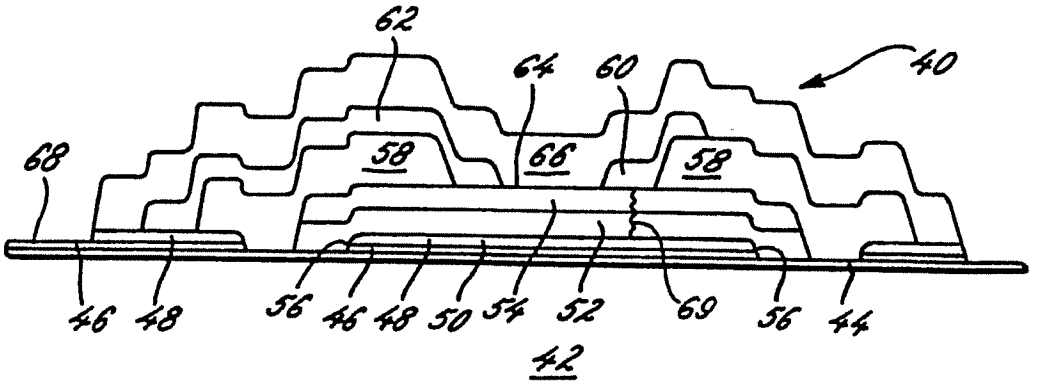


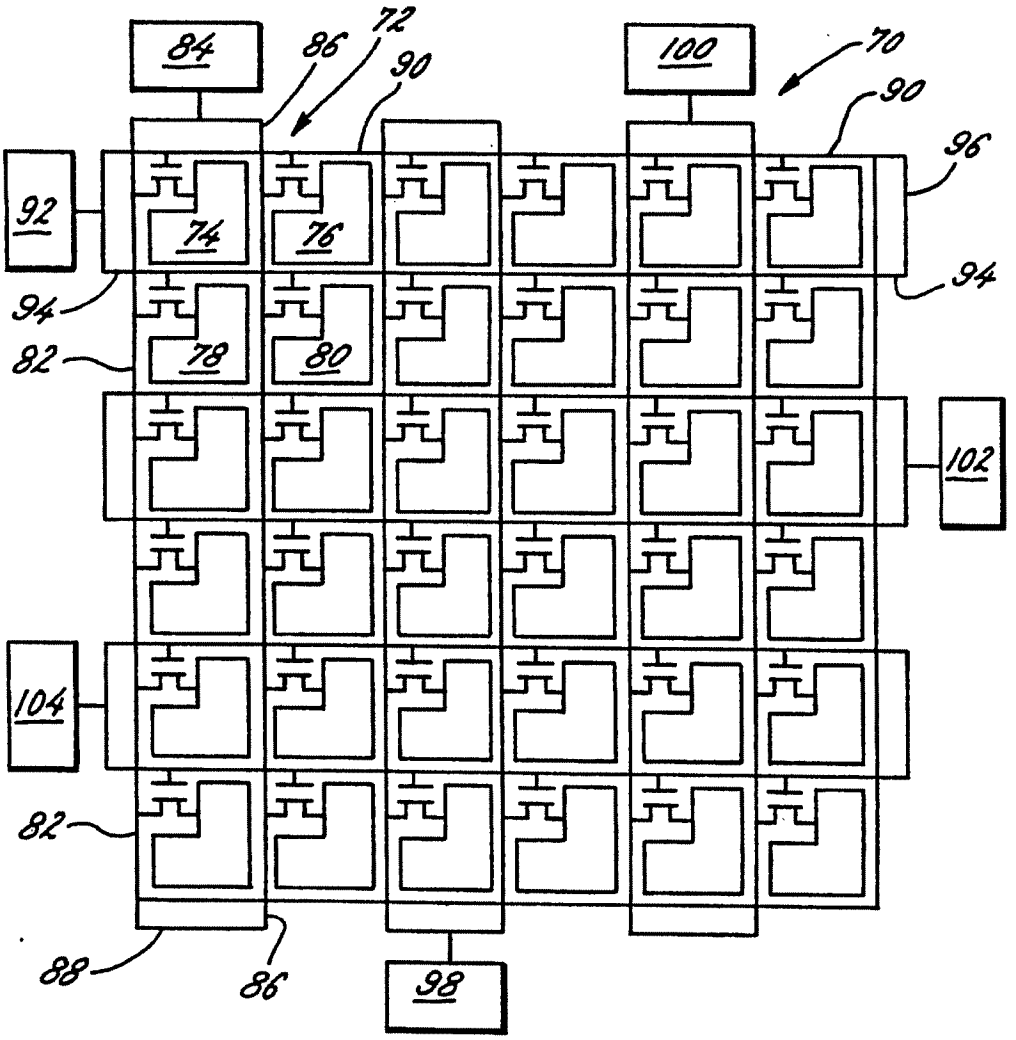
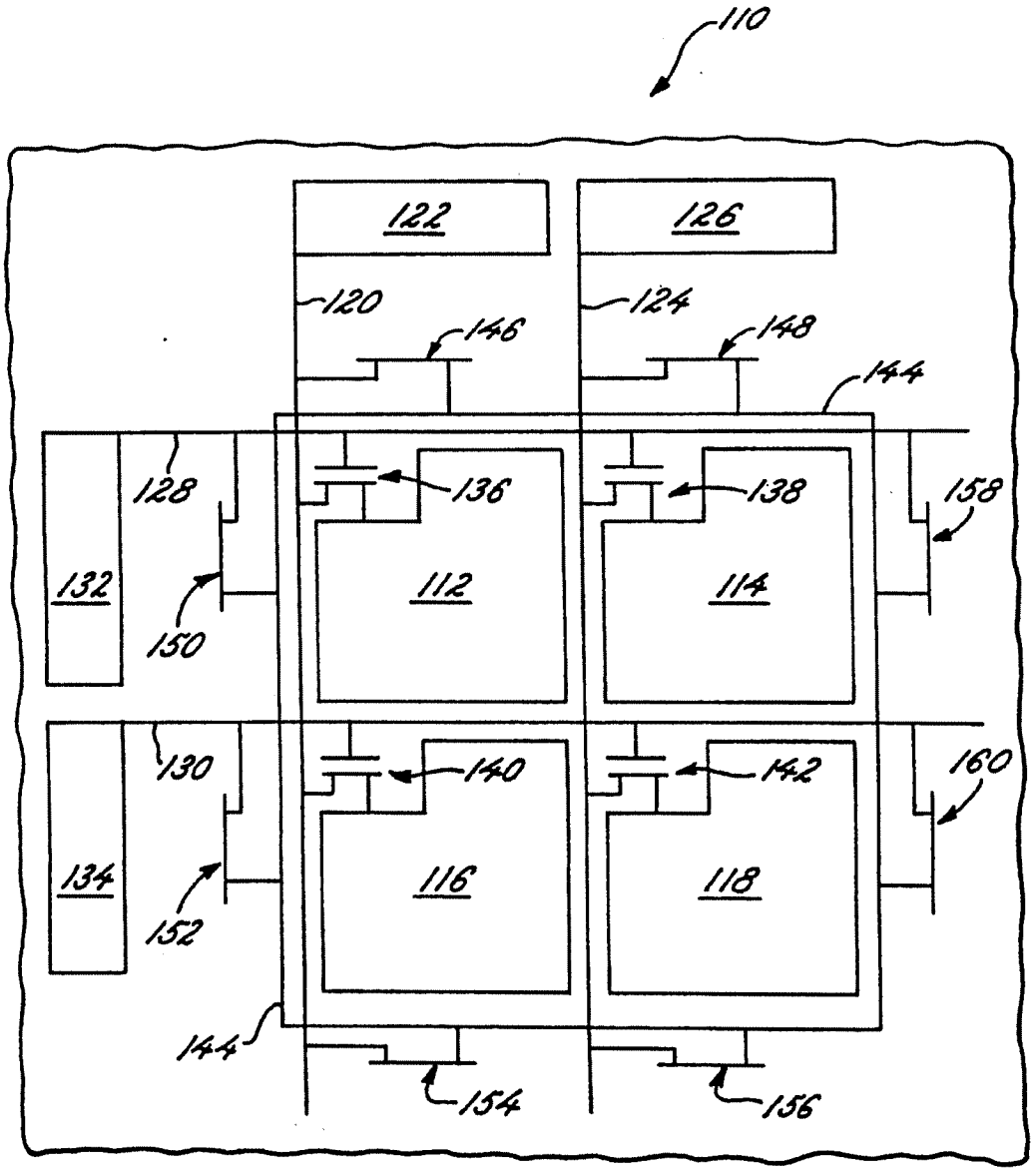


FIG. 4

FIG. 5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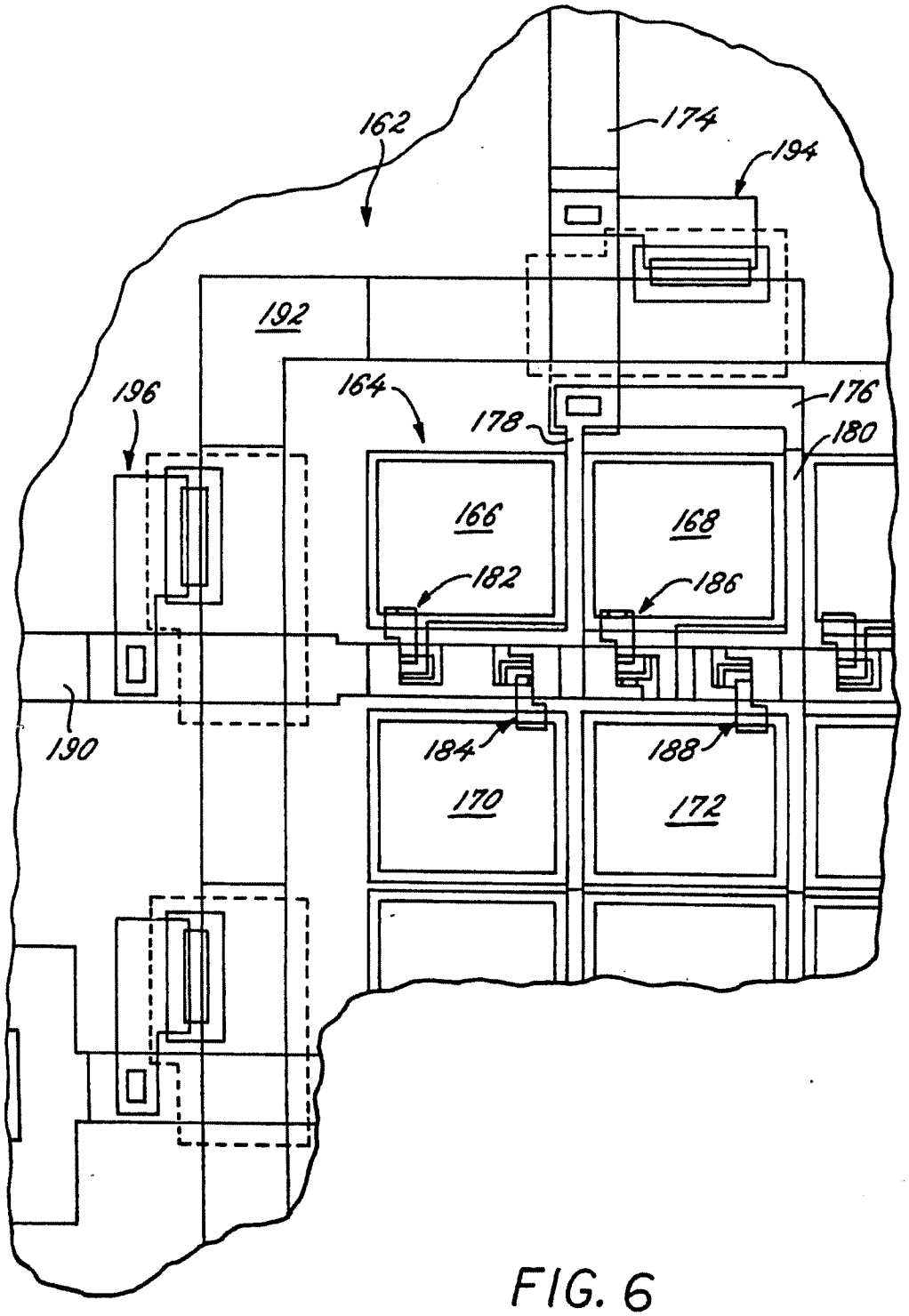
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FIG. 6

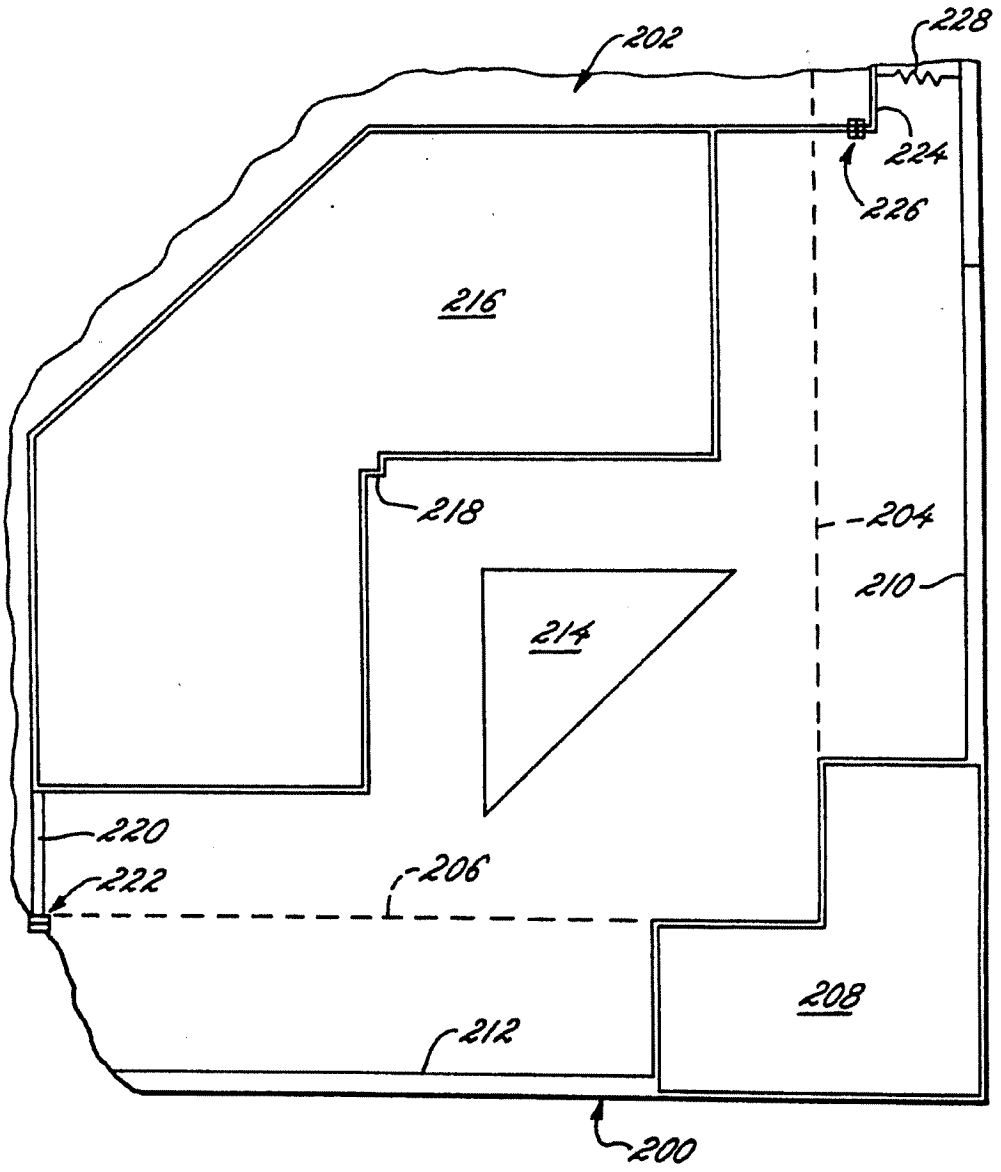

FIG. 7

METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY

BACKGROUND OF THE INVENTION

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

In recent years there has been growing interest in flat panel displays, such as those which employ liquid crystals, electrochromic or electroluminescence, as replacements for conventional cathode ray tubes (CRT). The flat panel displays promise lighter weight, less bulk and substantially lower power consumption than CRT's. Also, as a consequence of their mode of operation, CRT's nearly always suffer from some distortion. The CRT functions by projecting an electron beam onto a phosphor-coated screen. The beam will cause the spot on which it is focused to glow with an intensity proportional to the intensity of the beam. The display is created by the constantly moving beam causing different spots on the screen to glow with different intensities. Because the electron beam travels a further distance from its stationary source to the edge of the screen than it does to the middle, the beam strikes various points on the screen at different angles with resulting variation in spot size and shape (i.e. distortion).

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid crystal, electroluminescent or electrochromic materials such as zinc sulfide, a gas plasma of, for example, neon and argon, a dichroic dye, or such other appropriate material or device as will luminesce or otherwise change optical properties in response to the application of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

The circuitry for a flat panel display is generally designed such that the flat panel timeshares, or multiplexes, digital circuits to feed signals to one row and column control line of the pixels at a time. Generally one driving circuit is used for each row or column control line. In this way a subthreshold voltage can be fed to an entire row containing hundreds of thousands of pixels, keeping them all dark or inactive. Then a small additional voltage can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties. The pixels can be made to glow brighter by applying a larger voltage or current of a longer pulse of voltage or current. Utilizing liquid crystal displays (LCD's) with twisted nematic active material, the display is substantially transparent when not activated and becomes light absorbing when activated. Thus, the image is created on the display by sequentially activating the pixels, row by row, across the display. The geometric distortion described above with respect to CRT's is not a factor in flat panel displays since each pixel sees essentially the same voltage or current.

One of the major problems that arises with respect to the prior art method of manufacture of backplanes for active matrix displays (e.g. those employing thin film transistors at each pixel) is that they generally suffer production yield problems similar to those of integrated circuits. That is, the yields of backplanes produced are generally not 100% and the yield (percentage of backplanes with no defects) can be 0% in a worst case. High quality displays will not tolerate any defective pixel transistors or other components. Also, larger size displays are generally more desirable than smaller size displays. Thus, a manufacturer is faced with the dilemma of preferring to manufacture larger displays, but having to discard the entire product if even one pixel is defective. In other words, the manufacturer suffers a radically increased manufacturing cost per unit resulting from decreasing usable product yield.

One solution to the low yield problem is disclosed in U.S. Ser. No. 948,224, filed Dec. 31, 1986, now U.S. Pat. No. 4,676,761 entitled "Method of Manufacturing Flat Panel Backplanes Including Improved Testing and Yields Thereof and Displays Made Thereby", which is owned by the assignee of the present application and is incorporated herein by reference.

These problems of increased cost and decreased yield are improved in the present invention by providing methods of manufacturing display backplanes and the resulting displays with electrostatic discharge protection which provide protection against fatal defects during and after manufacture of the displays.

SUMMARY OF THE INVENTION

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter.

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view schematic representation of an active matrix display backplane made by a prior art method;

FIG. **2** is a cross-section of one transistor of the prior art backplane which could be utilized with the present invention;

FIG. **3** is a cross-section of one transistor which could be utilized with the present invention;

FIG. **4** is a plan view schematic representation of one prior embodiment of a subpixel matrix display;

FIG. **5** is a plan view schematic representation of a matrix display illustrating one embodiment of an internal ESD guard ring of the present invention;

FIG. **6** is an enlarged plan view of a portion of one embodiment of a subpixel matrix display illustrating the internal ESD guard ring in accordance with the present invention; and

FIG. **7** is a partial plan view of one embodiment of an exterior ESD guard ring of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. **1**, there is shown a schematic representation of an active matrix flat panel display device **10** made in accordance with conventional photolithographic techniques. One such device **10** and the manufacture thereof is more fully described in Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels, A. J. Snell, et al., *Applied Physics*, No. 24, p. 357, 1981. The device **10** includes a substrate **12**, sets of contact pads **14** and **16**, sets of control or bus lines **18** and **20**, and, in this particular example of the prior art, transistors **22** and pixel back contacts **24**.

The substrate **12** commonly employed in these devices is formed from glass. The control lines **18** and **20** are organized into a matrix of rows **18** and columns **20**. The control line rows **18** in this device **10** serve as gate electrodes and the control line columns **20** as source connections. One contact pad **14** is connected to one end of each of the row control lines **18**. One contact pad **16** is connected to one end of each of the column control lines **20**. The display drive control (not shown) is connected to the sets of pads **14** and **16**.

At each matrix crossover point **26**, where a row line **18** and a column line **20** cross, a switching element, transistor **22** is formed to connect the row line **18** and column line **20** to the pixel back contacts **24**. The active medium is deposited at least on the contacts **24** which will optically change properties in response to the combined voltages or currents in the respective crossover point **26** formed by the row **18** and column **20**. The active medium at a given crossover point **26** will appear as a square or dot in the overall checkerboard type matrix of the display **10**. The actual size of the transistors **22** and the contacts **24** are not now drawn to scale, but are shown schematically for illustration only.

It should be noted that theoretically there is no limit on the number of rows **18** and columns **20** that can be employed, only a portion of which are illustrated in FIG. **1**. Therefore, there is also no theoretical limit on the outside dimensions of such a device **10**. However, the present state of the lithographic art places a practical limit on the outside dimensions of these devices. The present alignment techniques generally allow high resolution display devices to be manufactured approximately five inches on a side **28**, although improved techniques of up to fourteen inches on a side has been demonstrated.

The problem encountered by the prior art method of manufacture is that if the array of device **10** contains any defective pixel transistors **22** or other circuit elements causing a pixel to be inoperative, it must be discarded.

Referring in detail to FIG. **2**, several problems occur when the switching element, transistor **22** is manufactured. The substrate **12** is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid crystal display manufacturers that the high sodium concentration can poison the liquid crystal materially diffusing through the overlying ITO layer and hence an SiO_2 suppression layer **30** is generally formed on the substrate **12**. There are some high quality low sodium types of substrates available, which would not need the suppression layer **30**. An ITO layer **32** is formed and etched to provide an ITO free area on which the gate **18** is deposited. Following the deposition of the gate **18**, a gate insulator layer **34** is deposited. Although a smooth uniform coverage of the gate **18** by the insulator **34** is illustrated, in production the gate **18** has or can have sharp edges which lead to pin holes or thinning of the insulator **34** at the gate edges. The source and drain metals can short to the gate **18**. The thinning or pin holes produce transistors **22**, which if operative, do not have uniform operating characteristics and hence the backplane is worthless.

One attempt to solve this problem, is to make the gate **18** very thin, but the resistivity is then too high to make the large arrays necessary for the backplane. A second attempt to solve the problem, is to make the gate insulator **34** very thick, but this decreases the gain of the transistor **22** and is also self defeating.

An amorphous silicon layer **36** is then deposited, with the source **20** and a drain **38** deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor **22**. During operation the activation of the source **20** and the gate **18** couples power through the silicon alloy **36** to the drain and hence to the contact pad **24** formed by the ITO layer **32**.

During manufacture of the device **10**, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines **18** and the source lines **20**. The discharge frequently will result in a short **39** through the insulator **34** or a short **39'** through the insulator **34** and the silicon layer **36** in the transistor **22**, between the adjacent crossover points of the lines **18** and **20** as can be seen in FIG. **2**. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device **10**, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device **10** does not provide any redundancy or subpixels and hence the defect cannot easily be isolated.

Referring now to FIG. **3**, there is shown a schematic representation of one embodiment of a transistor **40** which can be utilized with the present invention. The transistor is more fully disclosed in U.S. Pat. Nos. 4,545,112 and 4,736,229, which are incorporated herein by reference.

A glass substrate **42** includes a barrier SiO_2 layer **44** thereon. As above mentioned, a low sodium glass sub-

strate, such as Corning 7059 glass, could be utilized, and hence the barrier layer **44** can be eliminated. The detailed deposition steps are described in the above-referenced patent and application. An ITO layer **46** is deposited and then a refractory metal layer **48** is deposited on the ITO layer **46**.

The layers **46** and **48** are etched to form a gate electrode **50**. A gate insulator **52** and a semiconductor material **54** are sequentially deposited over the gate **50**. The material **54** preferably is an amorphous silicon alloy. To avoid the possibility of any gate to source or drain shorts at gate edges **56**, a dielectric **58** is deposited over the gate **55**, the gate insulator **52** and the semiconductor **54**. The dielectric **58** is deposited to a sufficient thickness to ensure that no shorts or thin spots are formed between the edges **56** of the gate **50** and a source **60** and a drain **62** deposited thereover.

The dielectric **58** is etched away only on a substantially planar central region **64** of the semiconductor layer **54**. This insures uniform operating characteristics for the transistors **40** in the backplane array. A passivating layer **66** is deposited over the whole structure to complete the structure of the transistor **40**.

During all of the transistor processing steps, the refractory metal layer **48** remains over a pixel contact pad **68** upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad **68** leaving the ITO layer **46** exposed after all the processing has been completed.

The gate to source or drain shorts referred to above in discussing the dielectric **58**, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric **58**, but will not be eliminated. The potential can be high enough to again form a short **69** through the gate insulator **52** and the semiconductor material **54** in the transistor **40**, between the source **60** and the gate **50**. Depending upon the display structure, at least one pixel or one subpixel (FIG. **4**) will be defective.

Referring now to FIG. **4**, a subpixel matrix display of the above-referenced application, U.S. Ser. No. 948,224, is designated generally by the reference numeral **70**. The subpixel matrix display **70** is illustrated as having each pixel subdivided into four subpixels, but the pixels could be subdivided into numerous other configurations such as two subpixels, two by four or six subpixels or in three subpixels for color applications. Each pixel **72** is subdivided into four subpixels **74**, **76**, **78** and **30** (only one pixel **72** is so numbered for illustration). As previously stated, the number of pixels is merely shown for illustration purposes and the display **70** could contain any desired number and configuration, square or rectangular.

A column (source) line or bus **82** connects the subpixels **74** and **78** and all other column subpixel pairs in one-half of each of the pixels to a column or source contact pad **84** at one edge of the display **70**. A second column (source) line or bus **86** connects the subpixels **76** and **80** and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad **84**. The bus lines **82** and **86** are interconnected (shorted) at or before the pad **84** and are interconnected (shorted) at the opposite ends by a line or short **88**.

A row (gate) line or bus **90** connects the subpixels **74** and **76** and all other row subpixel pairs in one-half of each of the pixels to a row (gate) pad **92**. A second row (gate) line or bus **94** connects the subpixels **78** and **80** and all other row subpixel pairs in one-half of each of the pixels to the row pad **92**. The bus lines **90** and **94** are interconnected (shorted) at or before the pad **92** and are interconnected (shorted) at the opposite ends by a line or short **96**.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads **98** and **100**, etc. The pads **84**, **98** and **100** are illustrated as being an opposite sides of the display to provide additional connecting space for the pads, however, they also could all be on one side as in the display **10**. Each of the other subpixel pairs also are connected in rows to respective row (gate) pads **102** and **104**, etc.

The pixel **72** then is divided into four subpixels **74**, **76**, **78** and **80** which allows for one of the subpixels to be defective, such as the subpixel **74**, without causing a fatal defect, since the remaining three subpixels **76**, **78** and **80** remain operative. In prior devices, the pixel **72** would be totally defective and hence the display **70** would be inoperable.

Further, one often fatal display defect is caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display **70**. With the respective subpixels pairs of row and column bus lines interconnected, however, an open in a bus line will at most cause one subpixel to be inoperative. An open in one or more of the bus lines between the subpixels will result in no defects, since the current is supplied from the opposite shorted end of the row or column bus line. Thus, the display **70** in effect has redundant row and column bus lines.

To avoid the fatal defect of the multiple open lines, as also disclosed in U.S. Ser. No. 948,224, the redundant row and column bus lines can be further interconnected at each subpixel. Each pair of the column bus lines **82** and **86** are additionally interconnected between each of the subpixels **74**, **78**, etc. by respective lines or shorts. In a like manner, each pair of the row bus lines **90** and **94** are interconnected between each of the subpixels **74**, **76**, etc. by respective lines or shorts. Further, although both the row bus lines and the column bus lines can be interconnected between each subpixel, only one of the row or the column bus line sets might be shorted to limit the loss of active pixel display area.

The short **69** in one of the active devices in the display **70** can be eliminated by opening the row or column line between the short and the line. This results in only one subpixel, such as the subpixel **74** being defective and due to the small size of the subpixel, is not a fatal defect (i.e. not readily visual). The rest of the corresponding column and row subpixels would be operable due to the redundant and interconnected row and column bus lines.

Referring now to FIG. **5**, a matrix display incorporating one embodiment of an internal ESD guard ring of the present invention is designated generally by the reference numeral **110**. The matrix display **110** is illustrated having four pixels **112**, **114**, **116** and **118**. The pixels, however, can be subdivided into numerous subpixel configurations such as two or four subpixels, two by four or six subpixels or in three subpixels for color display applications. Also, as previously stated for the

subpixel matrix display **70**, the number of pixels can be of any number and configuration, square or rectangular.

A column (source) line or bus **120** connects the pixels **112** and **116** and all other pixels in the same column to a source contact pad **122** at one edge of the display **110**. A source line **124** connects the pixels **114** and **118** to a source contact pad **126**. In a like manner, a pair of row (gate) lines **128** and **130** connect respective pairs of pixels **112**, **114** and **116**, **118** in each row to respective gate pads **132** and **134**.

Each pixel **112**, **114**, **116** and **118** includes a respective active element, such as transistors **136**, **138**, **140** and **142** which couple the pixels to the respective source lines **120** or **124** and gate lines **128** or **130**. To prevent a large electrostatic potential discharging through one of the transistors **136**, **138**, **140** and **142**, an internal ESD guard ring **144** is formed around the pixels **112**, **114**, **116** and **118**. The guard ring **144** is illustrated as a closed ring, but could also be an open L or C-shaped line if the gate and source pads all are on one respective side of the display **110**.

The ESD guard ring **144** also is coupled via respective transistors **146**, **148**, **150** and **152** to, the source and gate lines. The guard ring **144** will be coupled to the end of each source and gate line, so if the source and gate lines include pads at their opposite ends (not illustrated), then the guard ring **144** will include a further respective set of transistors **154**, **156**, **158** and **160**.

The ESD guard ring **144** preferably is formed from a low resistance metal, such as an aluminum alloy. The transistors **146** through **160** can include a floating gate (not illustrated), no gate, or can include an oxide below to form a spark gap.

In operation, with the guard ring **144**, a potential placed upon the source pads **122** will not short one of the transistors **136** or **140**. Instead, the transistor **146** will turn on followed by the transistor **150**, shorting the potential from the pad **122**, via the line **120**, the transistor **146**, the guard ring **144**, the transistor **150** and the line **128** to the pad **132**. Thus, the guard ring **144** will not allow high potentials across the pads **122**, **126**, **132** and **134**. The guard ring **144** preferably is formed concurrently with the display elements and is not removed, providing continuous protection even following manufacture of the display **110**.

A specific subpixel display incorporating an internal guard ring of the invention is best illustrated in FIG. **6** and is designated generally by the reference numeral **162**. The display **162** includes a plurality of pixels, each having four subpixels in a similar fashion to the display **70** illustrated in FIG. **4**. Only one pixel **164** is illustrated in detail and includes four subpixels **166**, **168**, **170** and **172**. A source line **174** includes a shorting line **176** which is connected to a pair of source lines **178** and **180**, coupled to each of the subpixels by a respective transistor structure **182**, **184**, **186** and **188**, which are not described in detail. The transistors **182**, **184**, **186** and **188** also couple the subpixels **166**, **168**, **170** and **172** to a gate line **190**.

An internal ESD guard ring **192** is coupled via a transistor structure **194** to the source line **174** and via a transistor structure **196** to the gate line **190**. The guard ring **192** and transistors **194** and **196** operate as before described to short any potential to ground. The low value of the normal operating voltages does not turn on the transistors **194** and **196**, which do not effect the normal display operation.

The ESD preventive structure can also include an outer ESD guard ring **200**, best illustrated in FIG. **7**. Only one corner portion **202** of the display and guard ring **200** is illustrated. While the display is being manufactured, the outer guard ring **200** is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines **204** and **206**. A corner pad **208** is connected to each other corner pad (not illustrated) by respective outer conductive lines **210** and **212** of the guard ring **200**. The L-shaped corner pad **208** can be grounded and also provides the alignment for the scribe lines **204** and **206**, which are utilized to disconnect the source and gate jumpers and the guard ring **200** after the structure is completed. The corner portion **202** includes a triangular pad **214** which provides alignment for diagonal corner displays, when utilized.

A backplane pickup contact pad **216** also is provided, which includes a corner **218** for aligning the backplane with the front plane. The pad **216** includes a shunt line **220** which is connected to one set of source or gate lines via a shunt transistor **222** along the edge to be scribed and removed along the line **206**. The line **210** is connected to the other set of gate or source lines by a shunt line **224**, a shunt transistor **226** and a large resistance **228**, such as 100 K ohms (illustrated schematically). The outer ESD guard ring **200** provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance **228** provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line **210** and the other set of gate or source lines. The resistance **228** minimizes the discharge current surge and the shunt transistors **222** and **226** act as before described. There will be at least one corner backplane pickup pad **216** and preferably there will be two or three, each with their associated shunt transistors.

The outer guard ring lines **210** and **212** preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring **44** and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines **204** and **206** can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

Modification and variations of the present invention are possible in light of the above teachings. The transistors **22** or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material **54**, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors **146**, **194** and **222**, etc. also can be formed as other active switching elements, such as diodes. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

2. The method as defined in claim **1** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

3. The method as defined in claim **2** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

4. The method as defined in claim **3** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

5. The method as defined in claim **3** including forming a corner on said pad to align the front plane and back plane of the display.

6. The method as defined in claim **3** including forming a plurality of pickup pads, each one on a separate corner of the display.

7. The method as defined in claim **1** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

8. The method as defined in claim **1** including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

9. The method as defined in claim **8** including forming separate shunt switching elements between said inner guard ring and each row and column line.

10. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines; and

forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

11. The method as defined in claim **10** including forming separate shunt switching elements between said inner guard ring and each row and column line.

12. The method as defined in claim **10** including interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another and forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

13. The method as defined in claim **12** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

14. The method as defined in claim **13** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

15. The method as defined in claim **14** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

16. The method as defined in claim **14** including forming a corner on said pad to align the front plane and back plane of the display.

17. The method as defined in claim **10** including forming a plurality of pickup pads, each one on a separate corner of the display.

18. The method as defined in claim **10** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

19. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines, substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another; and

an outer removable electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

20. The backplane as defined in claim **19** including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

21. The backplane as defined in claim **20** including at least one pickup pad coupled to said resistance via a shunt switching element.

22. The backplane as defined in claim **21** including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

23. The backplane as defined in claim **21** including a corner formed on said pad to align the front plane and back plane of the display.

24. The backplane as defined in claim **21** including a plurality of pickup pads, each one formed on a separate corner of the display.

25. The backplane as defined in claim **19** including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

26. The backplane as defined in claim **19** including an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

27. The backplane as defined in claim **26** including separate shunt switching elements formed between said inner guard ring and each row and column line.

28. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines; and

an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

29. The backplane as defined in claim 28 including separate shunt switching elements formed between said inner guard ring and each row and column line.

30. The backplane as defined in claim 28 including substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another and an outer electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

31. The backplane as defined in claim 30 including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

32. The backplane as defined in claim 31 including at least one pickup pad coupled to said resistance via a shunt switching element.

33. The backplane as defined in claim 32 including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

34. The backplane as defined in claim 32 including a corner formed on said pad to align the front plane and back plane of the display.

35. The backplane as defined in claim 28 including a plurality of pickup pads, each one formed on a separate corner of the display.

36. The backplane as defined in claim 28 including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,019,002

DATED : May 28, 1991

INVENTOR(S) : Scott H. Holmberg

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 2, lines 30-31, change "4,676,761" to --4,820,222--;

Col. 4, line 15, change "materially" to --material by--;

Col. 5, line 53, change "30" to --80--;
line 59, change "aIl" to --all--;

Col. 7, line 23, delete the third comma;

Col. 8, line 41, change "firs:" to --first--.

Signed and Sealed this

Twenty-third Day of February, 1993

Attest:

STEPHEN G. KUNIN

Attesting Officer

Acting Commissioner of Patents and Trademarks

EXHIBIT B

US005825449A

United States Patent [19]

Shin

[11] Patent Number: 5,825,449

[45] Date of Patent: Oct. 20, 1998

[54] **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Woo Sup Shin**, Kyungsangbuk-do, Rep. of Korea

[73] Assignee: **LG Electronics, Inc.**, Seoul, Rep. of Korea

[21] Appl. No.: **781,188**

[22] Filed: **Jan. 10, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 616,291, Mar. 15, 1996.

[30] **Foreign Application Priority Data**

Aug. 19, 1995 [KR] Rep. of Korea 25538/1995

[51] **Int. Cl.**[6] **G02F 1/136**; G02F 1/1343; G02F 1/1345

[52] **U.S. Cl.** **349/148**; 349/149; 349/43

[58] **Field of Search** 349/149, 148, 349/43, 139, 152, 147

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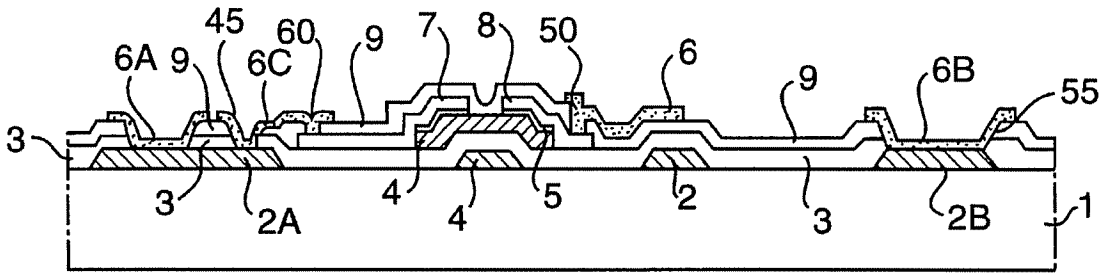
Primary Examiner—William L. Sikes
Assistant Examiner—Tiep H. Nguyen
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

11 Claims, 5 Drawing Sheets



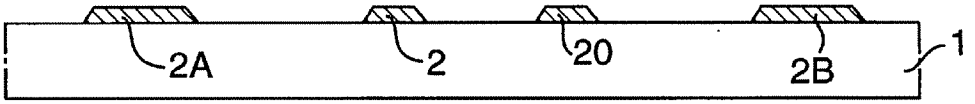


FIG. 1a
PRIOR ART

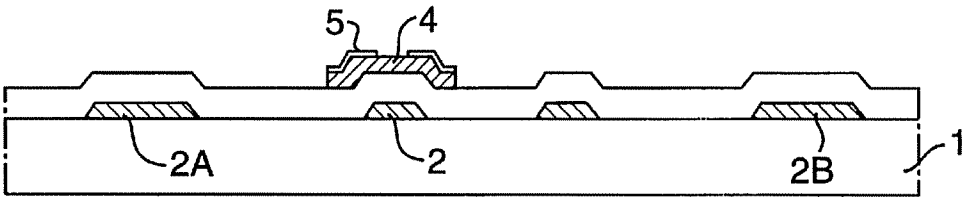


FIG. 1b
PRIOR ART

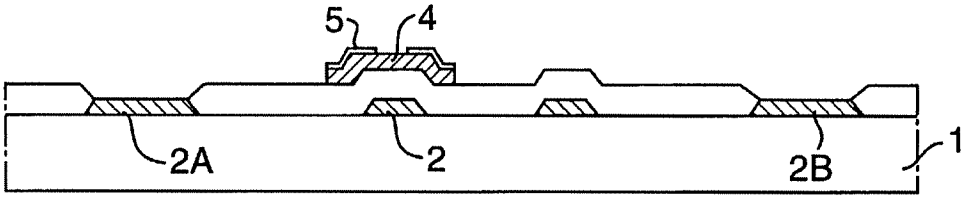


FIG. 1c
PRIOR ART

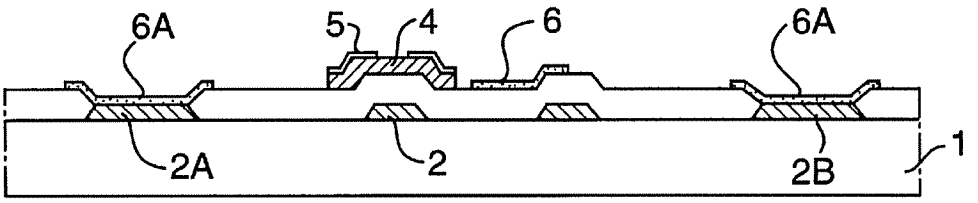


FIG. 1d
PRIOR ART

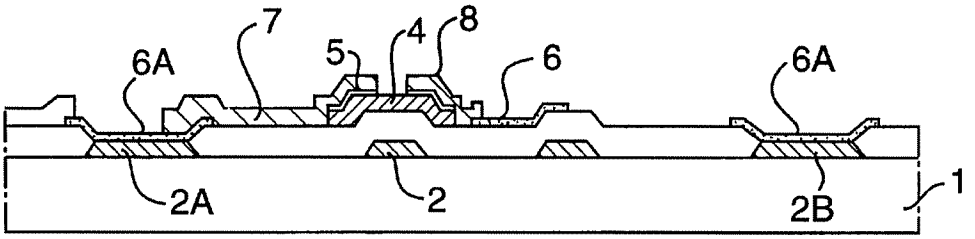


FIG. 1e
PRIOR ART

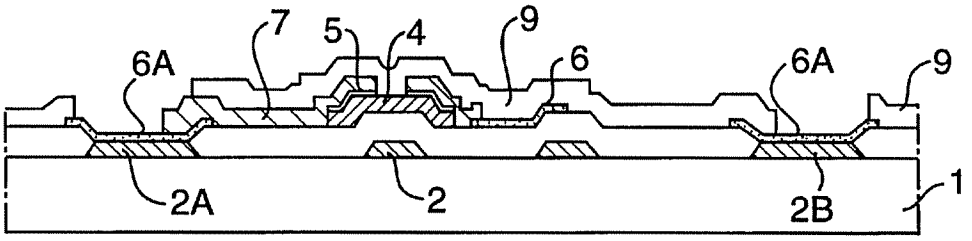


FIG. 1f
PRIOR ART

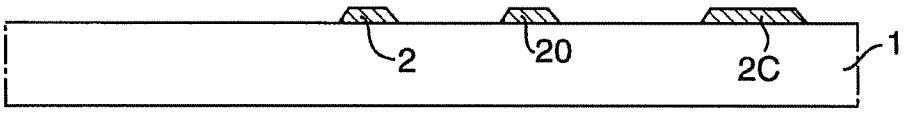


FIG. 2a

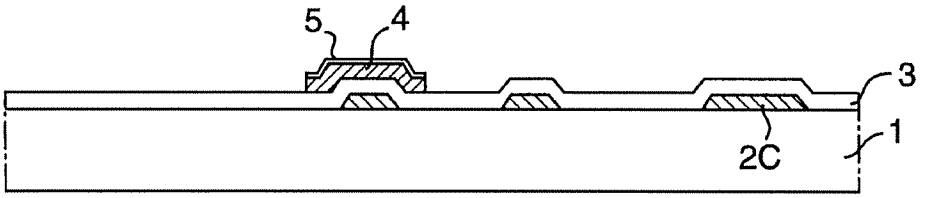


FIG. 2b

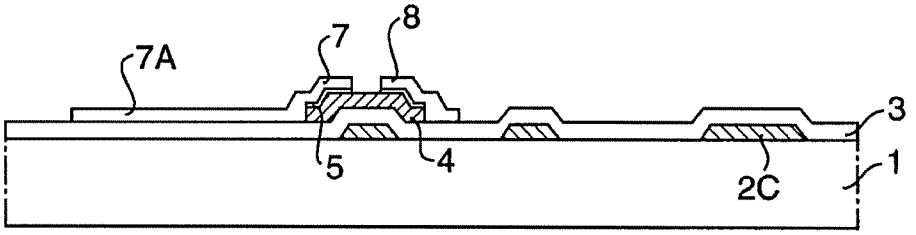


FIG. 2c

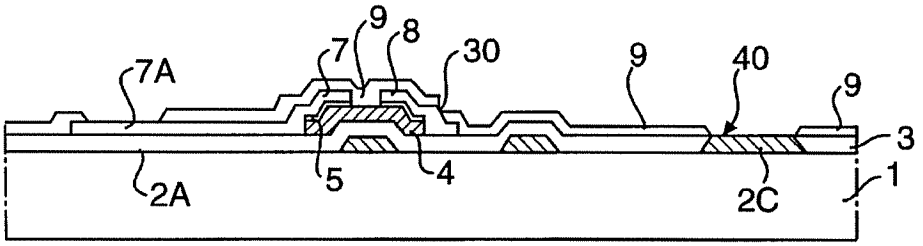


FIG. 2d

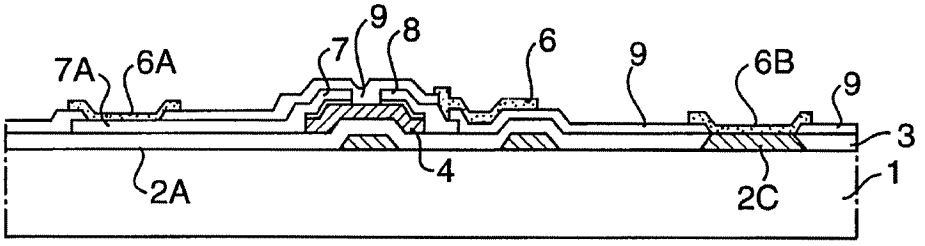


FIG. 2e

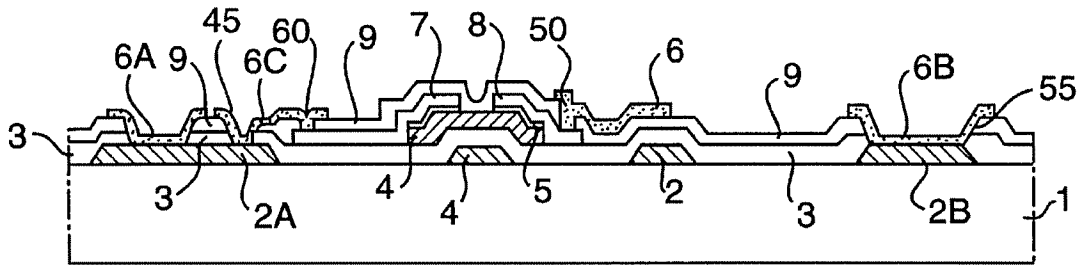


FIG. 3

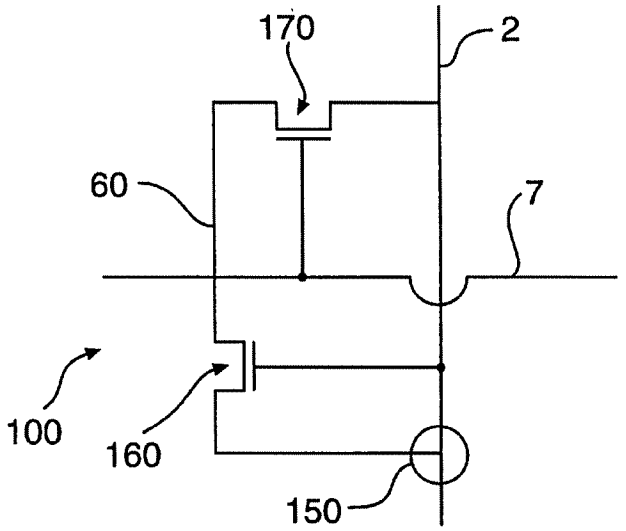


FIG. 4

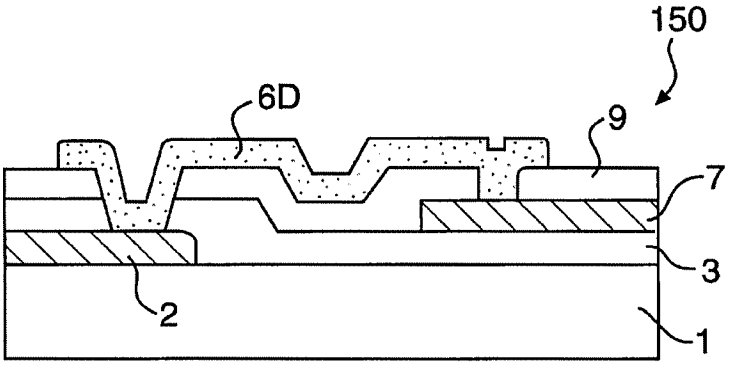


FIG. 5

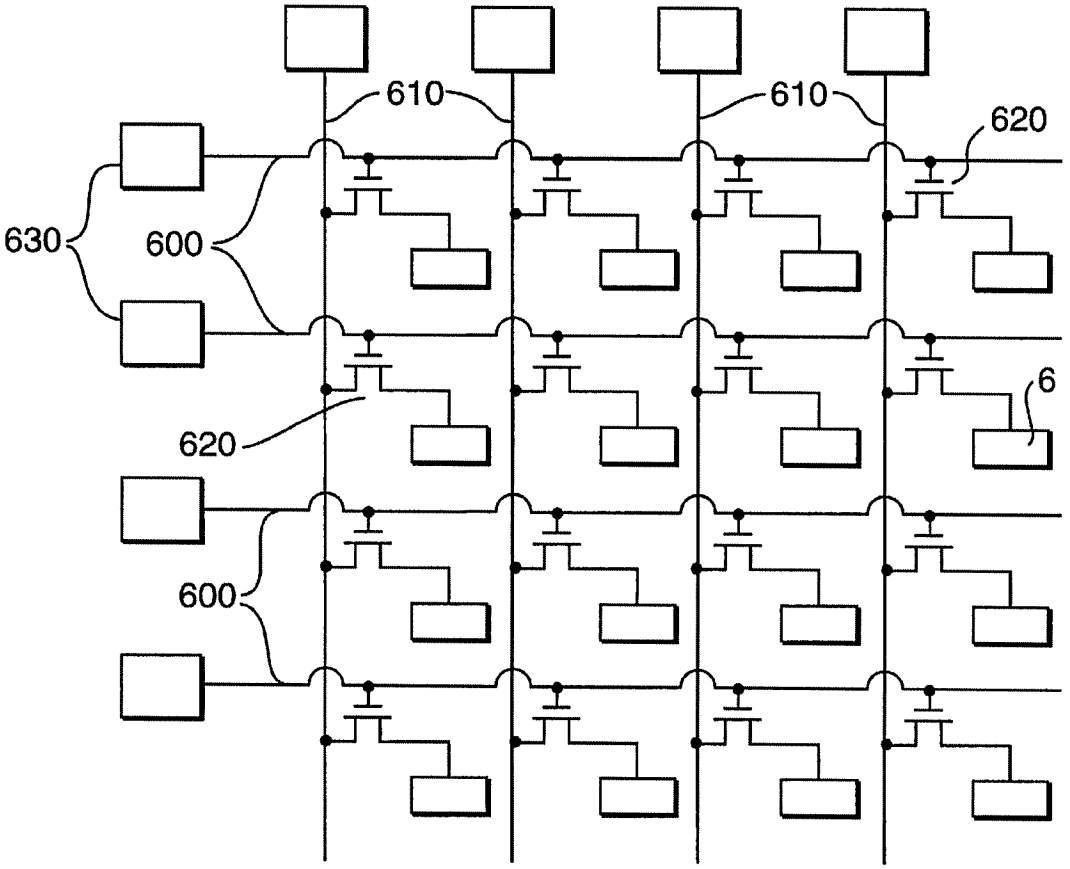


FIG. 6
PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a continuation of application Ser. No. 08/616,291, Filed Mar. 15, 1996.

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display (LCD) device and a method of manufacturing the same, and more particularly, to a liquid crystal display device having a combined source electrode and source pad structure.

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. **6**, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode **6** disposed on a bottom plate. The bottom plate further includes a plurality of gate lines **600** intersecting a plurality of data lines **610**.

Thin film transistors **620**, serving as active devices, are located at intersecting portions of gate lines **600** and data lines **610**. Gate lines **600** and data lines **610** are connected to the gates and sources, respectively of thin film transistors **620**. In addition, pixel electrodes **6** are connected to respective drain electrodes of thin film transistors **620**. Gate Pads **630** and Data Pads **640** are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. **1***a*–**1***f*.

As shown in FIG. **1***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, storage capacitor electrode **2**D, source pad **2**A, and gate pad **2**B. Gate pad **2**B is used for receiving a voltage to drive and active layer in the completed TFT device.

As shown in FIG. **1***b*, a gate insulating film **3**, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate **2**. An amorphous silicon active layer **4** is formed on a portion of gate insulating film **3** overlying gate **2**. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer **5** is formed on amorphous silicon layer **4** as an ohmic contact layer. Doped semiconductor layer **5** and amorphous silicon layer **4** are then etched in accordance with a predetermined active layer pattern.

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film **3** is selectively etched to expose source pad **2**A and gate pad **2**B (see FIG. **1***c*). Next, as shown in FIG. **1***d*, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode **6**, which is formed on a portion of the display pixel, while ITO patterns **6**A and **6**B are formed on source pad **2**A and gate pad **2**B, respectively.

As shown in FIG. **1***e*, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes **7** and **8**, respectively. Source electrode **7** is connected to source pad **2**A, and drain electrode **8** is contact with impurity-doped semiconductor layer **5** and pixel electrode **6**. In the completed device structure, source electrode

7 conducts a data signal, received from a data wiring layer and drain electrode **8**, to pixel electrode **6**. The signal is stored in the form of charge on pixel electrode **6**, thereby driving the liquid crystal.

As shown in FIG. **1***f*, a nitride film is deposited on the entire surface of the substrate as a passivation layer **9** in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer **9** is selectively etched to expose source-pad **2**A and gate pad **2**B, thereby completing the TFT.

In the conventional method described above, The source electrode **7** and pixel electrode **6** provided on the same surface of gate insulating film **3**. Accordingly, processing errors can cause these electrodes to contact each other. As a result, shorts can occur, thereby reducing yields.

Further, since the source pad for the source wiring is composed of the same material as the gate, its contact resistance with the underlying source electrode can be high. In addition, at least six masking steps are required as follows: patterning the gate, storage capacitor electrode, source pad and gate pad; forming the active layer pattern; patterning the gate insulating film for exposing the pad part; forming the pixel electrode; forming the source and drain electrode; and patterning the passivation film for exposing the pad part. Thus, the conventional process requires an excessive number of fabrication steps which increase cost and further reduce yield.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems, it is an objective of the present invention to provide a liquid crystal display device and a method of manufacturing the same, in which processing errors can be prevented and the Yield can be increased by etching the gate insulating film after the step of forming the passivation layer.

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. **1***a* to if are cross-sectional views illustrating steps of a conventional method for manufacturing a liquid crystal display device;

FIGS. **2***a* to **2***e* are cross-sectional views illustrating steps of a method for manufacturing a liquid crystal display according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view illustrating a liquid crystal display device structure according to a second embodiment of the present invention;

FIG. **4** is a circuit diagram of one example of a liquid crystal display device in which a gate material is connected with a source material in accordance with a third embodiment of the present invention; and

FIG. **5** is a vertical-cross-sectional view of the device shown in FIG. **4**.

FIG. **6** is a plan view schemetic representation of one prior embodiment of a matrix display.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings.

Referring first to FIG. **2***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form a gate electrode **2**, a storage capacitor electrode **2**D, and a gate pad **2**C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

As shown in FIG. **2***b*, a gate insulating film **3** such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate **2**. Semiconductor active layer **4** is then formed on insulating gate **2**. Active layer **4** is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer **5** is formed on amorphous silicon layer **4**, as an ohmic contact layer. Impurity-doped semiconductor layer **5** and amorphous silicon layer **4** are etched according to a predetermined active layer pattern.

As shown in FIG. **2***c*, a conductive layer for forming source electrode **7** and drain electrode **8** is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer **5** are exposed and then etched. Source electrode **7** thus forms part of a transistor region and serves as source pad **7**A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT.

As shown in FIG. **2***d*, a passivation layer **9**, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer **9** and gate insulating film **3** are selectively etched to form first, second and third contact holes **20**, **30** and **40**, thereby exposing a predetermined region of source pad **7**A above gate insulating film **3**, a predetermined region of drain electrode **8**, and a predetermined region of gate pad **2**C. For external electrical connections It is necessary to exposed pads **7**A and **2**C.

As shown in FIG. **2***e*, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode **6**. As further shown in FIG. **2***e*, pixel electrode **6** is connected to the upper portion of drain electrode **8** At the same time, ITO pattern **6**B is formed on gate pad **2**C. In addition, ITO pattern **6**A is provided on source pad **2**A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad **2**C, layer **6**B and layer **6**A, source pad **7**A is thus completed.

As described above, the pixel electrode **6** is formed after the passivation process in the present invention. In contrast, pixel electrode **6** is formed after the pad process or the source/drain formation process in the conventional method. Thus, the passivation layer is interposed between the source/drain formation material and the pixel electrode, thereby effectively isolating these layers and preventing shorts.

Further, unlike the conventional process, the method in accordance with the present invention does not require the step of exposing the pad directly after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process. Thus, the pixel electrode, which is made of ITO, is formed on the source and gate pads. In addition, the source pad is not formed of gate material, but is formed from the source formation material, while the source and drain are deposited. Thus, the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided.

FIG. **3** illustrates a second embodiment of the present invention in which the step of etching the gate insulating layer and the step of etching the passivation layer to expose the pads are preformed in only one mask step. In particular, source pad **2**A is composed of gate material, as in the conventional method, and is formed at the same time as gate **2**, storage capacitor electrode **2**D and gate pad **2**B. After forming first, second, third and fourth contact holes **45**, **50**, **55** and **60**, material for forming the pixel electrode is then deposited. As a result, since both the first (**45**) and fourth (**60**) contact holes are formed over source pad **2**A (formed of the same material as the gate) and source electrode **7**, respectively, the source electrode **7** and source pad **2**A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer **6**C connects source electrode **7** with source pad **2**A, and a second transparent conductive layer **6** (i.e., the pixel electrode) is connected to drain electrode **8**.

In other words, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, a storage capacitor electrode **2**D,. a source pad **2**A and a gate

pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode 6 connected to drain electrode 8 through the contact hole overlying drain electrode 8 in the pixel part. At the same time, ITO patterns 6A, 6B and 6C are formed to contact source pad 2A and gate pad 2B through the contact holes formed at gate insulating film 3 and passivation layer 9.

Further, in accordance with an additional embodiment of the present invention, a repair line or static electricity protection circuit can also be provided during deposition of the pixel electrode layer. FIG.4 is a schematic diagram of static electricity protection circuit 100, and FIG.5 is an enlarged cross-sectional view of a portion 150,of the circuit.

In the circuit shown in FIG.4. if a high potential due to an electrostatic discharge is present on source electrode 7, for example, transistor 170 is rendered conductive to discharge source electrode 7 to gate line 2. Similarly, gate line 2 can discharge to source electrode 7 via transistor 160. As shown in FIG.5, the connection between gate line 2 and source electrode 7 is achieved by forming contact holes in insulative films 3 and 9 and then depositing conductive material (preferabel ITO) into these holes while forming the pixel electrode.

According to the present invention as described above, the manufacture of the TFT of the liquid crystal display device can be accomplished using five mask steps (step of forming the gate, step of forming the active layer, step of forming the source and drain, step of etching the passivation layer and gate insulating film, and step of forming the pixel electrode), while the conventional process requires six or more mask steps. Thus, manufacturing cost can be reduced.

Further, when the source pad is formed from the same material as the source electrode, the contact resistance problem caused when the source pad is in contact with the source electrode can be solved. In addition, since the pixel electrode is formed after forming the passivation layer, processing errors resulting in the pixel electrode contacting the source and drain can be prevented.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

3. A wiring structure in accordance with claim 2, wherein said third conductive layer includes indium tin oxide.

4. A wiring structure in accordance with claim 2, wherein said first and second via holes constitute a common hole exposing said exposed portion of said first conductive layer, a sidewall of said common hole being substantially smooth.

5. A wiring structure in accordance with claim 2, wherein said second via hole is aligned with said first via hole.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

7. A liquid crystal display device in accordance with claim **6**, wherein said third conductive layer includes material suitable for forming a pixel electrode.

8. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively.

9. A method of manufacturing a liquid crystal display device in accordance with claim **8**, wherein said selective etching step is performed in a single etch step and said third conductive layer includes indium tin oxide.

10. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including:
a gate electrode,
a gate pad, and
a source pad;

a gate insulating film on said surface of said substrate,

a portion of said gate insulating film overlying said gate electrode;

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer;

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

* * * * *

EXHIBIT C

United States Patent [19]

Shimbo

[11] **Patent Number: 4,624,737**

[45] **Date of Patent: Nov. 25, 1986**

[54] **PROCESS FOR PRODUCING THIN-FILM TRANSISTOR**

[75] Inventor: **Masafumi Shimbo, Tokyo, Japan**

[73] Assignee: **Seiko Instruments & Electronics Ltd., Tokyo, Japan**

[21] Appl. No.: **743,092**

[22] Filed: **Jun. 10, 1985**

[30] **Foreign Application Priority Data**

Aug. 21, 1984 [JP] Japan 59-173848

[51] **Int. Cl.**[4] **H01L 21/306; B44C 1/22; C03C 15/00; C23F 1/02**

[52] **U.S. Cl.** ..... **156/643;** 29/576 R; 29/578; 29/591; 156/652; 156/653; 156/656; 156/657; 156/659.1; 156/662; 156/667; 357/4; 357/23.1; 427/88; 427/93; 427/94

[58] **Field of Search** ..... 156/643, 646, 652, 653, 156/655, 656, 657, 659.1, 661.1, 662, 667, 668; 204/192 E, 192 EC; 427/38, 39, 88, 89, 90, 93, 94, 95; 430/313, 317, 318; 29/571, 576 R, 578, 591; 357/4, 23.1, 23.7, 65, 71

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Primary Examiner—William A. Powell
Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

4 Claims, 13 Drawing Figures

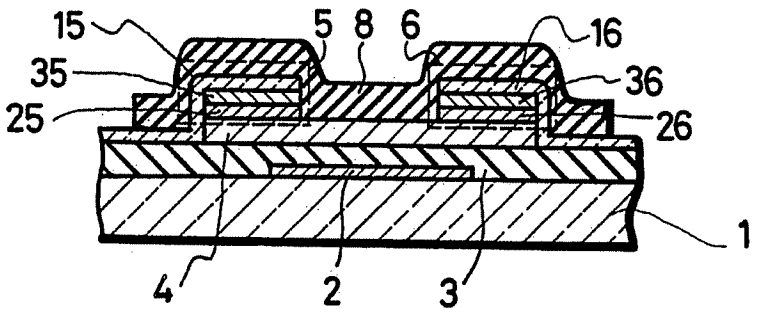


FIG. 1a PRIOR ART

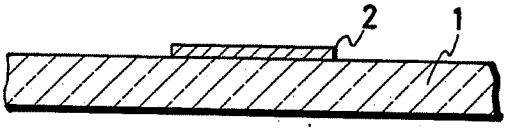


FIG. 1b PRIOR ART

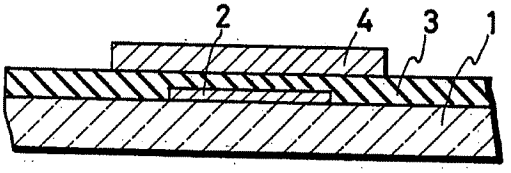


FIG. 1c PRIOR ART

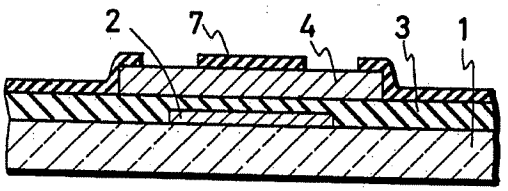


FIG. 1d PRIOR ART

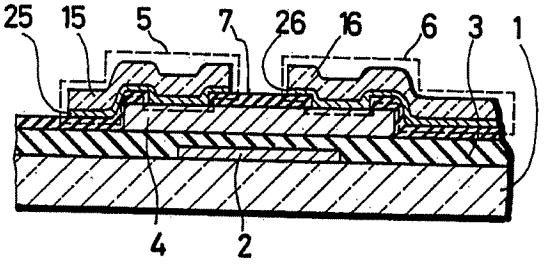


FIG. 2a

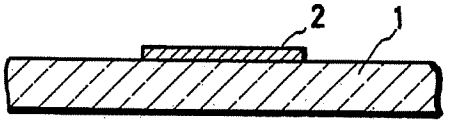


FIG. 2b

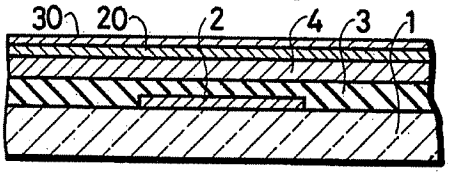


FIG. 2c

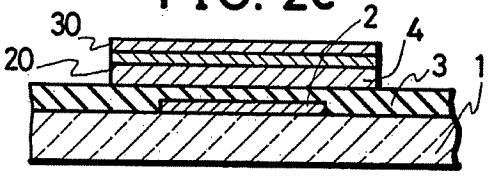


FIG. 2d

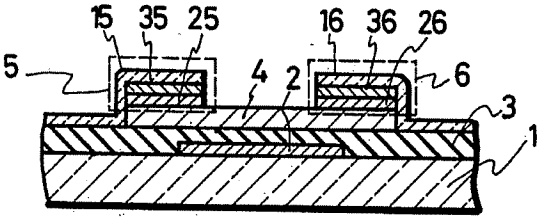


FIG. 2e

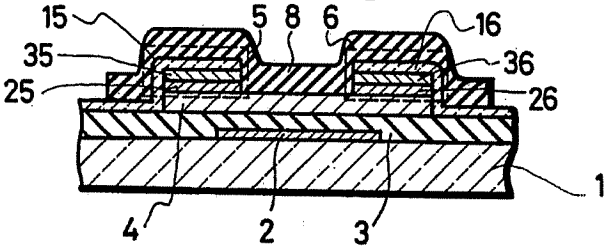


FIG. 3a

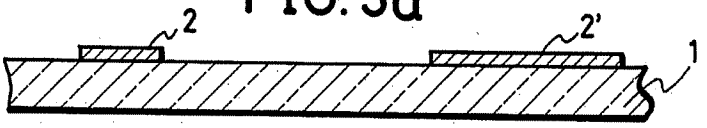


FIG. 3b

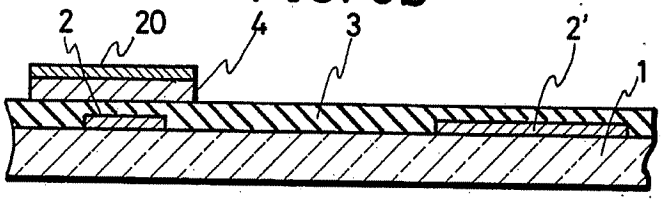


FIG. 3c

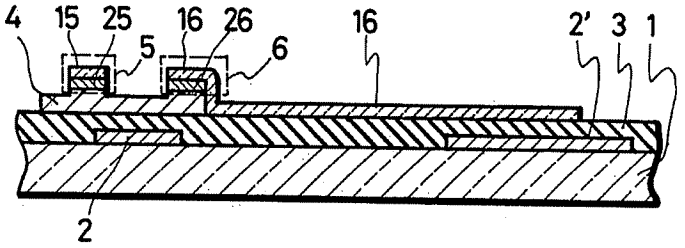
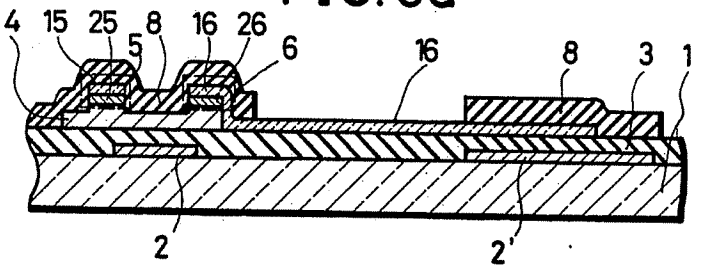


FIG. 3d



PROCESS FOR PRODUCING THIN-FILM TRANSISTOR

BACKGROUND OF THE INVENTION

This invention relates to a process for producing a thin-film transistor with improved performance.

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. **1***a* to **1***d* illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. **1***a* in a sectional view is the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as a glass substrate. Then, as shown in FIG. **1***b*, a gate insulating film **3** (such as silicon nitride film) and an amorphous silicon film **4** are continuously deposited, and said amorphous silicon film **4** is selectively etched. Then a field insulating film **7** (such as SiOx film) is deposited and windows for contact with source and drain regions are formed as shown in FIG. **1***c*. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. **1***d*, for instance n^+ amorphous silicon films **25**, **26** and metal (such as Al) films **15**, **16** are deposited and selectively etched to form drain and source electrodes **5**, **6**, thereby completing a thin-film transistor unit. If necessary, a surface passivation film and/or light-shielding film are further formed thereon.

In the conventional process shown in FIGS. **1***a* to **1***d*, since the masking step precedes the deposition of n^+ amorphous films **25**, **26**, natural oxide is produced on the exposed surface of amorphous silicon film **4**. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to exhibit its desired characteristics. A similar phenomenon would also occur at the interface of n^+ amorphous silicon films **25**, **26** and metal films **15**, **16**.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* to **1***d* are sectional views showing the sequential steps in a conventional thin-film transistor production process.

FIGS. **2***a* to **2***e* are sectional views illustrating stepwise a process for producing a thin-film transistor according to the present invention.

FIGS. **3***a* to **3***d* are sectional views illustrating the sequential steps for producing a thin-film transistor according to the process of this invention as it was applied to a substrate for liquid crystal display.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. **2***a* to **2***e* are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. **2***a* shows in a sectional view the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode **2**.

In the next step illustrated in FIG. **2***b* in a sectional view, a gate insulating film **3**, a high-resistivity film **4**, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film **20** and a conducting film **30** made of a metal or other material are successively formed on said gate electrode **2** and substrate **1** without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film **3** from a mixed gas of SiH_4 and NH_3, forming a high-resistivity a-Si:H film **4** by using SiH_4 and forming a n^+ a-Si:H film **20** from a mixed gas of PH_3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film **30** can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film **3**. In place of said high-resistivity amorphous silicon film **4**, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF_4, or a microcrystalline amorphous silicon film. Such alloys can be also used for said low-resistivity amorphous silicon film **20**, and such film may contain other impurites beside phosphorous impurities. As said conducting film **30**, it is desirable to use a stable conducting film such as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like. Use of a transparent conducting film has the advantage that the process is simplified when the thin-film transistor of this invention is applied to an active matrix liquid crystal display.

FIG. **2***c* illustrates the step in which said conducting film **30**, low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. **2***d* in a sectional view, drain and source electrode members **15**, **16** are selectively provided, and conducting film **30** and low-resistivity amorphous silicon film **20** shown in FIG. **2***c* are selectively removed with said electrode members **15**, **16** serving at least as a part of the mask to form drain electrode **5** and source electrode **6**. In this step, it is desirable to clean the surface of conducting film **30** by proper etching means such as sputter etching or ion

etching before forming said drain and source electrode members **15, 16**. In this case, the channel areas of the thin-film transistor are safe from damage by cleaning as they are covered with conducting film **30**. The same materials as used for conducting film **30** and other materials such as Al can be used for said drain and source electrode members **15, 16**. When selectively etching low-resistivity amorphous silicon film **20**, no problem arises even if it is overetched to the extent that etching reaches the high-resistivity amorphous silicon film **4**.

In the final step illustrated in FIG. 2*e*, a surface passivation film **8** is deposited, and the drain and source electrodes **15, 16** and gate electrode **2** are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said surface passivation film **8**. If light shielding is required, a multilayer film composed of said insulating film and a metal or high-resistivity semiconductor film can be used as said surface passivation film **8**. When amorphous silicon-germanium alloy ($a\text{-}Si_{1-x}Ge_x$) is used as light-shielding film, surface passivation may not be necessary.

FIGS. 3*a* to 3*d* show sectionally a unit picture cell in an application of the present invention to the manufacture of a TFT substrate for liquid crystal display. FIG. 3*a* illustrates a step in which gate electrode **2** extending along one line and gate electrodes **2'** on another line are formed on a transparent insulating substrate **1** such as glass substrate. Then, as illustrated in FIG. 3*b*, gate insulating film **3**, high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20** are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region in the area where a thin-film transistor is to be formed.

In the next step illustrated in FIG. 3*c*, a transparent conducting film such as ITO film is deposited; then, drain electrode **15** and source electrode **16** which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film **20** is removed. In this example, a charge-holding capacitor is formed by said picture cell electrode (source electrode) **16**, gate electrode **2'** and gate insulating film **3**. In the final step shown sectionally in FIG. 3*d*, surface passivation film **8** concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode **15** and a part of gate electrodes **2, 2'** (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film **20**, but a conducting film such as ITO film may be formed on said low-resistivity film **20** as in the example shown in FIG. **2**.

As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20**, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film **20** and conducting film **30**. Further, since the interfaces of low-resistivity amorphous silicon film **20** or conducting film **30** and drain and source electrodes **15, 16** can be cleaned without damaging the high-resistivity amorphous silicon film, a good contact can be obtained without sacrificing the inherent properties of thin-film transistor.

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

While the present invention has been principally described regarding an embodiment thereof as applied to the production of a thin-film transistor using amorphous silicon by utilizing plasma CVD, the invention can as well be applied to the manufacture of thin-film transistors using semiconductor films by utilizing the photo CVD or molecular beam and/or the ion beam deposition method, thin-film transistors using polysilicon, and thin-film transistors using semiconductor films of other materials than silicon; consequently, the present invention is of great industrial significance.

I claim:

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

2. A process for producing a thin-film transistor according to claim **1**, wherein in said second step said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film, and both of said films are continuously deposited without being exposed to the oxidizing atmosphere.

3. A process for producing a thin-film transistor according to claim **1** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

4. A process for producing a thin-film transistor according to claim **2** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

* * * * *

CIVIL COVER SHEET

The JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

I.(a) PLAINTIFFS

LG.PHILIPS LCD CO., LTD.

DEFENDANTS

CHI MEI OPTOELECTRONICS CORPORATION; AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; TATUNG COMPANY; TATUNG COMPANY OF AMERICA, INC.; AND VIEWSONIC CORPORATION

(b) County Of Residence Of First Listed Plaintiff Republic of Korea

County Of Residence Of First Listed Defendant Republic of China (Taiwan)

(c) Attorneys (Firm Name, Address And Telephone Number)

Richard D. Kirk (rk0922)
The Bayard Firm
222 Delaware Avenue, Suite 900
P.O. Box 25130
Wilmington, DE 19899-5130
(302) 655-5000

Attorneys (If Known)

II. BASIS OF JURISDICTION (PLACE AN "X" IN ONE BOX ONLY)

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question (U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place An 'X' In One Box For Plaintiff And One Box For Defendant)
(For Diversity Cases Only)

	DEF			DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business in this State	☐ 4 ☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business in Another State	☐ 5 ☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6 ☐ 6

IV. NATURE OF SUIT *PLACE AN "X" IN ONE BOX ONLY)*

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Property Liability

TORTS

PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury Med. Malpractice
- ☐ 365 Personal Injury Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

FORFEITURE/PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 RR & Truck
- ☐ 650 Airline Regs
- ☐ 660 Occupational Safety/Health
- ☐ 690 Other

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 420 Banks and Banking
- ☐ 450 Commerce/ICC Rates/etc.
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of I Information Act
- ☐ 900 Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes
- ☐ 890 Other Statutory Actions

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 444 Welfare
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence

HABEUS CORPUS:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt Relations
- ☐ 730 Labor/Mgmt Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl Ref Inc Security Act

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U S. Plaintiff or Defendant)
- ☐ 871 IRS Third Party 26 USC 7609

V. ORIGIN

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from State Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION (Cite The U.S. Civil Statute Under Which You Are Filing And Write Brief Statement Of Cause. Do Not Cite Jurisdictional Statutes Unless Diversity)

35 U.S.C. §§101 et seq. THE PATENT STATUTE

VII. REQUESTED IN COMPLAINT CHECK IF THIS IS A **CLASS ACTION** UNDER F.R.C.P. 23 **DEMAND $**

CHECK YES only if demanded in complaint
JURY DEMAND: ☒ YES ☐ NO

RELATED CASE(S) (See instructions)
LG.Philips LCD Co., Ltd. v. Tatung Company, et al., JUDGE The Honorable Joseph J. Farnan, Jr. DOCKET NUMBERS 05-292-JJF

DATE December 1, 2006

SIGNATURE OF ATTORNEY OF RECORD
/s/ RICHARD D. KIRK (RK0922)

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RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____

AO FORM 85 RECEIPT (REV. 9/04)

United States District Court for the District of Delaware

06 -- 726

Civil Action No. _____

ACKNOWLEDGMENT OF RECEIPT FOR AO FORM 85

NOTICE OF AVAILABILITY OF A UNITED STATES MAGISTRATE JUDGE TO EXERCISE JURISDICTION

I HEREBY ACKNOWLEDGE RECEIPT OF 6 COPIES OF AO FORM 85.

12/1/06
(Date forms issued)

(Signature of Party or their Representative)

Ben Lougheed
(Printed name of Party or their Representative)

Note: Completed receipt will be filed in the Civil Action